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Self-Organization of $CrSi_2$ Nanoislands on Si(111) and Growth of Monocrystalline Silicon with Buried Multilayers of $CrSi_2$ Nanocrystallites

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The process of self-organization of $CrSi_2$ nanosize islands on Si(111)7 × 7 surface has been investigated during reactive deposition (RDE) of Cr at 500 °C by methods of low energy diffraction (LEED) and differential reflectance spectroscopy (DRS). Morphology of grown samples has been studied by atomic force microscopy (AFM). DRS data have demonstrated the semiconductor nature of silicide islands from the beginning of Cr deposition at 500 °C. The optimal temperature (750 °C) and optimal Si thickness (50 nm) have been determined for silicon molecular epitaxy (MBE) growth atop $CrSi_2$ nanosize islands. Monolithic silicon–silicide heterostructures with multilayers of $CrSi_2$ nanosize crystallites have been grown.

Keywords: Silicon, Chromium Disilicide, Islands, Epitaxial Growth, Nanocrystallites, Monolithic Heterostructures.

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1. INTRODUCTION

Chromium disilicide ($CrSi_2$) is a narrow band gap semiconductor ($E_g = 0.35$ eV),[1] which has been epitaxially grown on Si(111) substrates.[2,3] Two type orientations have been observed for the $CrSi_2$ (0001)/Si(111) system: the A-type ((0001) $[11\bar{2}0]$ $CrSi_2$ // (111) $[11\bar{2}]$ Si) having the lattice mismatch with silicon 0.1%[4]) and the B-type ((0001) $[11\bar{2}0]$ $CrSi_2$ // (111) $[10\bar{1}]$ Si) having the lattice mismatch with silicon of about 16%.[5] In $CrSi_2$ (0001) A-type epitaxial films grown on Si(111)[6] a strong increase of hole mobility, decrease of hole concentration and a changing of carrier scattering mechanism have been observed, that corresponds to considerable alterations in their band structure. So a change of thermoelectric force in $CrSi_2$ epitaxial films also can be waited. But epitaxial growth of $CrSi_2$ (0001) B-type also has been obtained by template method[7] for thin films. Its have relaxed form with dislocation net.[8] But silicon has been epitaxially grown atop thin epitaxial $CrSi_2$ films.[9] Therefore, both types of $CrSi_2$ films are interesting for growth of double heterostructures and electrical applications in silicon planar technology.

The growth of chromium disilicide in the form of low dimension objects, for example in the form of nanosize crystallites (10–40 nm) in silicon lattice, can lead to interesting electrical, thermoelectrical and optical properties of such kind of objects. The quantum size effect will be observed under the essential decreasing of $CrSi_2$ crystallite sizes (4–6 nm[10]) that results in quantization of energy levels and increase of effective band gap value. The last can lead to an alteration of fundamental transition type: indirect—direct for $CrSi_2$. In the case of burying of quantum size $CrSi_2$ crystallites (Q0D system) with high density (10^{10}–10^{11} cm^{-2}) in the silicon crystalline lattice one could expect the considerable alterations of optical, electrical, photoelectrical and thermoelectrical properties of such nanocrystalline material.

Scanning tunneling microscopy (STM) study[11] of initial stages of reactive deposition epitaxy of Cr on Si(111)7 × 7 surface has shown a formation of nanosize chromium silicide islands of unknown composition up to 0.1 monolayer coverage and gradual transition to growth of $CrSi_2$ island at increase of Cr coverage. It was shown that the surface between chromium disilicide islands is partially or fully destroyed that connects with an introduction of silicon in the silicidation zone due to surface diffusion. The growth of $CrSi_2$ islands on Si(111)7 × 7 surface during Cr deposition at 500 °C has been studied by LEED and electron energy loss spectroscopy (EELS) at Cr deposition rate about 0.1 nm/min.[10] The formation of 3D nanosize $CrSi_2$ islands has been demonstrated at Cr thickness lower than 0.27 nm (1 nm Cr corresponds on Si(111) surface to 1.25 monolayer (Ml) or $9.75 \cdot 10^{14}$ cm^{-2}). However the growth

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of silicon on such surface has not been early studied and silicon heterostructures with buried chromium disilicide nanocrystallites have not been grown.

In this work the formation conditions of $CrSi_2$ nanosize islands on Si(111)7×7 surface were determined by low energy electron diffraction and differential reflectance spectroscopy methods. The epitaxial growth of silicon layers atop $CrSi_2$ nanosize islands were studied by LEED. An atomic force microscopy (AFM) was used for morphology investigations of grown silicon layers and multilayer structures.

2. EXPERIMENTAL DETAILS

Experiments were carried out in two ultra high vacuum (UHV) cambers. Optical properties of samples were studied in UHV chamber "VARIAN" with base pressure of $2 \cdot 10^{-10}$ Torr equipped with AES and differential reflectance spectroscopy (DRS) facilities.[12] The surface structure of grown samples was studied in the second UHV chamber ($P_b = 1 \cdot 10^{-9}$ Torr) equipped with LEED optics.

Samples for both chambers were cut from Si(111) substrates of n-type conductivity and 1Ω· cm resistivity. The silicon cleaning procedure was as follows: annealing at 700 °C during 4–5 hours, cooling during 12 hours, fleshes at 1250 °C (5 times on 1 second). Surface purity was controlled by AES method in first UHV chamber and by LEED method in another chamber. After the preparation procedure, the silicon surface showed the bright Si(111)7×7 LEED pattern. LEED patterns were registered with a digital camera in the manual mode. Chromium was deposited on hot (500 °C) silicon substrate from the annulled Ta tube in the thickness range of 0.01–0.18 nm (0.125–2.25 Ml). Silicon layers were deposited atop chromium disilicide islands from a rectangle-shaped silicon sublimation source heated with direct current. Chromium and silicon deposition rates were controlled by quartz sensor. It was about 0.017 nm/min (0.021 Ml/min) for Cr in all experiments. Silicon deposition rate was about 4 nm/min (20.8 Ml/min on Si(111) substrate).

DRS spectra were registered in the energy range of 1.1–2.8 eV during the Cr deposition. Reflectance spectra were recorded during every 12–14 seconds. The basic value, which is used in DRS method, is the differential reflectance coefficient (DRC), which is calculated relatively reflectance spectra of atomically clean silicon surface. Detailed descriptions of DRS method and registration scheme of DRS spectra were considered elsewhere.[12] The photon energy dependence of DRC contains in itself information about energies and probabilities of optical transitions in studied film or on the interface.[13]

Silicon film growth was performed by MBE method in the temperature range of 650–750 °C. In experiments the silicon film thickness was changed in the range of 20–50 nm. After the determination of optimal growth conditions of $CrSi_2$ islands and silicon covering layers (substrate temperature and silicon thickness) a growth of multilayer structures with buried $CrSi_2$ nanocrystallites was performed. Morphology of grown samples was studied *ex-situ* by atomic force microscopy (AFM) method on the multimode probe microscope Solver P47.

3. RESULTS AND DISCUSSION

Let us consider DRS data (Fig. 1(a)), which present in the form of differential reflectance coefficient spectra (DRC-spectra) at different Cr thickness. It is seen that already on the first stage of Cr deposition (0.0168 nm or 0.2 Ml) the 1.3, 1.7, 2.3, and 2.6 eV peaks are appeared in DRC-spectrum. These peaks are close to interband optical transitions in the energy band structure of $CrSi_2$ (1.3, 1.7, 2.1, and 2.5 eV[1]) at energies higher than 1 eV. The thickness dependence of RDC (Fig. 1(b)) shows a non-monotonous character that does not permit to use a method of dynamic standard[10] for a calculation of changes of

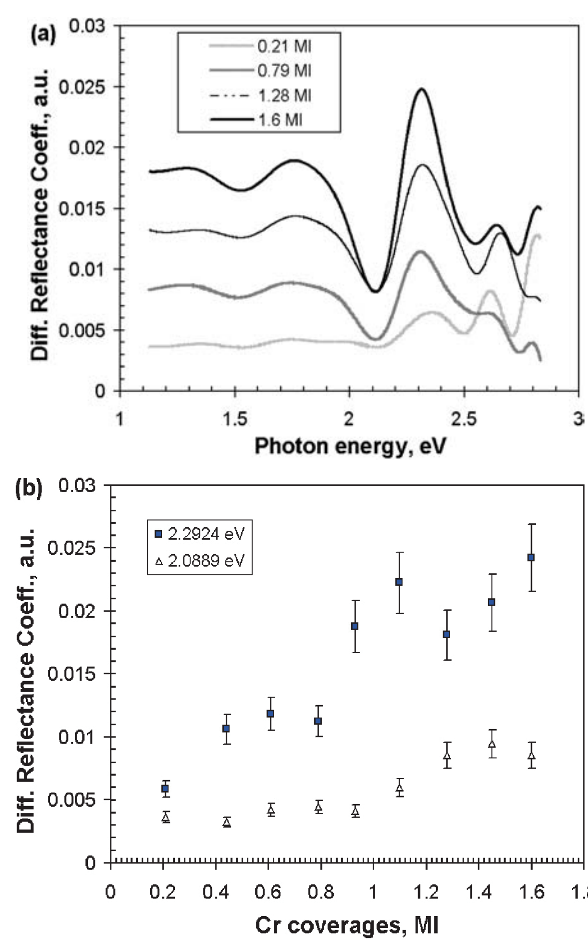

Fig. 1. (a) RDC dependence from Cr thickness layer at selected photon energies; (b) RDC spectra, registered at different Cr thicknesses (in Ml) during the RDE growth process at substrate temperature of 500 °C.

imaginary part of the dielectric function for a system of $CrSi_2$ islands on silicon substrate. However, one cannot see any metallic character (a decrease of DRC with increase of photon energy[14]) of DRC-spectra (Fig. 1(a)) at energies less than 1.5 eV. So, one can assert that islands of semiconductor chromium disilicide begin form from the Cr thickness of about 0.0168 nm (or 0.2 Ml), and a formation of metallic silicides is not observed. Since the DRC-value changes (Fig. 1(a)) insignificantly at thicknesses 0.20–0.80 Ml (0.0168–0.065 nm, first "plateau"), so this correspond to a nucleation of two-dimensional (2D) $CrSi_2$ islands on Si(111)7×7 surface and its growth in sizes and heights and formation of 3D $CrSi_2$ islands with some height distribution. This mechanism correlates with STM data[11] of Cr deposition on Si(111) at 450–500 °C, when different 2D and 3D islands have been formed on silicon surface at Cr coverages 0.1–1.0 Ml. At higher Cr thicknesses (1.0–1.6 Ml or 0.08–0.125 nm) a formation of the second "plateau" (Fig. 1(b)) and valuable increase of DRC-value in DRS-spectra (Fig. 1(a)) were observed. This region corresponds to a lateral overgrowth of 3D $CrSi_2$ islands without its corresponding height increasing.

For a study of surface morphology after 3D $CrSi_2$ island formation the sample with 0.07 nm (or 0.9 Ml) of Cr thickness was grown at 500 °C. Near circle form $CrSi_2$ islands with density $(4–5)\cdot10^9$ cm^{-2}, heights of 0.5–3.0 nm and lateral sizes of 30–50 nm were formed (Fig. 2(a)) on the silicon surface by AFM data. Surface filling was about 17–18%. About 72% of islands have height from 1 to 2 nm. Only 14% of $CrSi_2$ islands have height from 2 to 3 nm. When a chromium thickness increases up to 0.12 nm (1.5 Ml, Fig. 2(b)) the density and distribution of islands height are near the same, but its lateral sizes increases up to 50–100 nm. Islands have the ellipsoidal form with near the same orientation in respect to the substrate. An occupied island area increases up to 25–26%. Therefore, during the continuation of Cr deposition an increase of

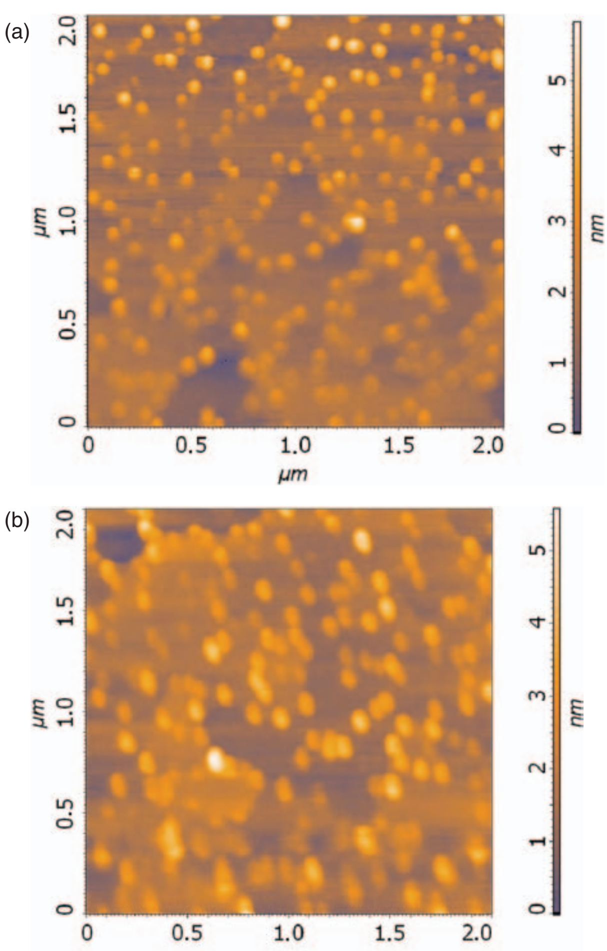

Fig. 2. AFM images for samples with different Cr thickness deposited at 500 °C on Si(111)7×7: (a) 0.07 nm (0.9 Ml) and (b) 0.12 nm (1.5 Ml).

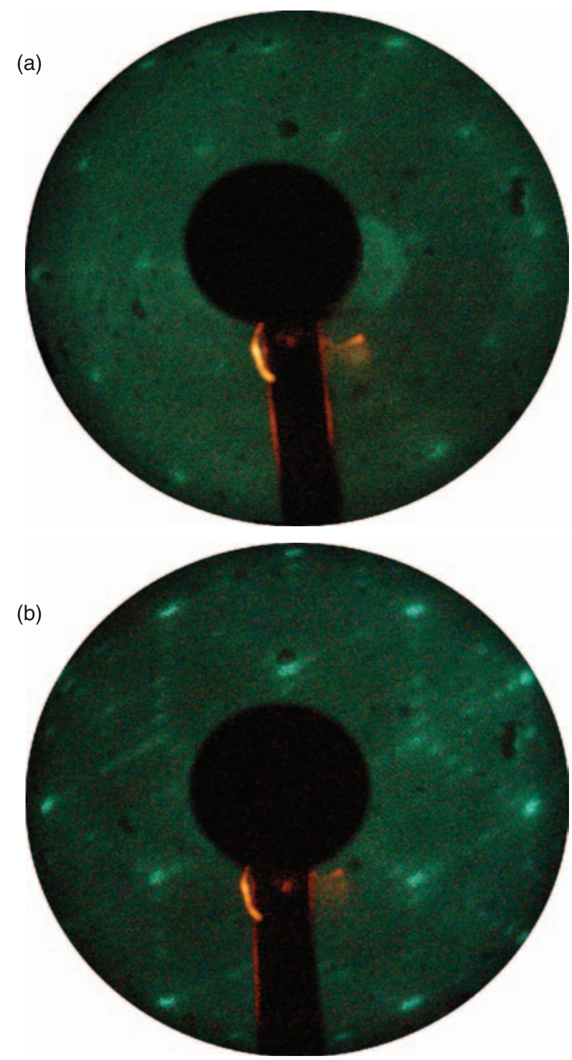

Fig. 3. LEED patterns ($E_p = 104$ eV) from—silicon surface with grown $CrSi_2$ islands (0.07 nm Cr, $T_{Si} = 500$ °C) (a) and from epitaxial silicon layer atop these $CrSi_2$ islands (b).

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differential reflectance coefficient (Fig. 1(b)) is determined by increase of area occupied by $CrSi_2$ islands.

Since the Cr deposition rate in our experiments was essentially lower (in 6 times) than in first growth experiments on $CrSi_2$ island formation on Si(111)[10] during RDE-process, so the conditions of island formation would be changed. The two-dimensional growth mechanism of $CrSi_2$ on silicon at higher deposition rate (0.12 Ml/min[10]) has been observed up to 0.27 nm. Only after that 3D $CrSi_2$ islands have been formed. In our experiments the boundary value of Cr thickness is essentially lower (0.065 nm or 0.8 Ml). What is a possible reason of such Cr boundary thickness decrease? When a Cr deposition rate increases then a density of $CrSi_2$ nucleus increases too and islands mainly grow in lateral sizes. At lower deposition rate nucleus density decreases, but a formation of $CrSi_2$ second layer is increased by silicon surface diffusion. Chromium thickness 0.07 nm corresponds to the formation of 0.21 nm of $CrSi_2$ or near the one $CrSi_2$ (0001) monolayer[1] on silicon (111) surface. We can propose that in grown $CrSi_2$ nucleus firstly only one monolayer of $CrSi_2$ formed on silicon. After that the formation of second and others $CrSi_2$ layers begins on island surface. Since the $CrSi_2$ islands cover only 18% of silicon surface, so the average thickness in 3D $CrSi_2$ islands is near 6 monolayers in the [0001] direction of $CrSi_2$ crystalline lattice or 3 $CrSi_2$ lattice constants in this direction.[1] This correlates with obtained AFM data (Fig. 2(a, b)), since the thickness of $CrSi_2$ islands changes only by based on an analysis of AFM and DRS data we have concluded that at critical Cr thickness (0.06–0.07 nm) a formation of 3D $CrSi_2$ islands with some height distribution occurs.

For a growth of nanosize $CrSi_2$ crystallites in silicon crystalline matrix the Cr thickness of 0.07 nm (0.9 Ml) was selected. This corresponds to the formation of 3D $CrSi_2$ islands with a small square on silicon surface.

Investigations of the influence of substrate temperature on the silicon growth (50 nm) atop $CrSi_2$ nanosize islands have carried out at three temperatures (650, 700, and 750 °C). By LEED data after the formation of $CrSi_2$ nanosize islands on the silicon surface a $Si(111)1\times 1$ pattern with increased background (Fig. 3(a)) was observed that corresponds by AFM data to the partial disordering of silicon surface between $CrSi_2$ islands due to involvement

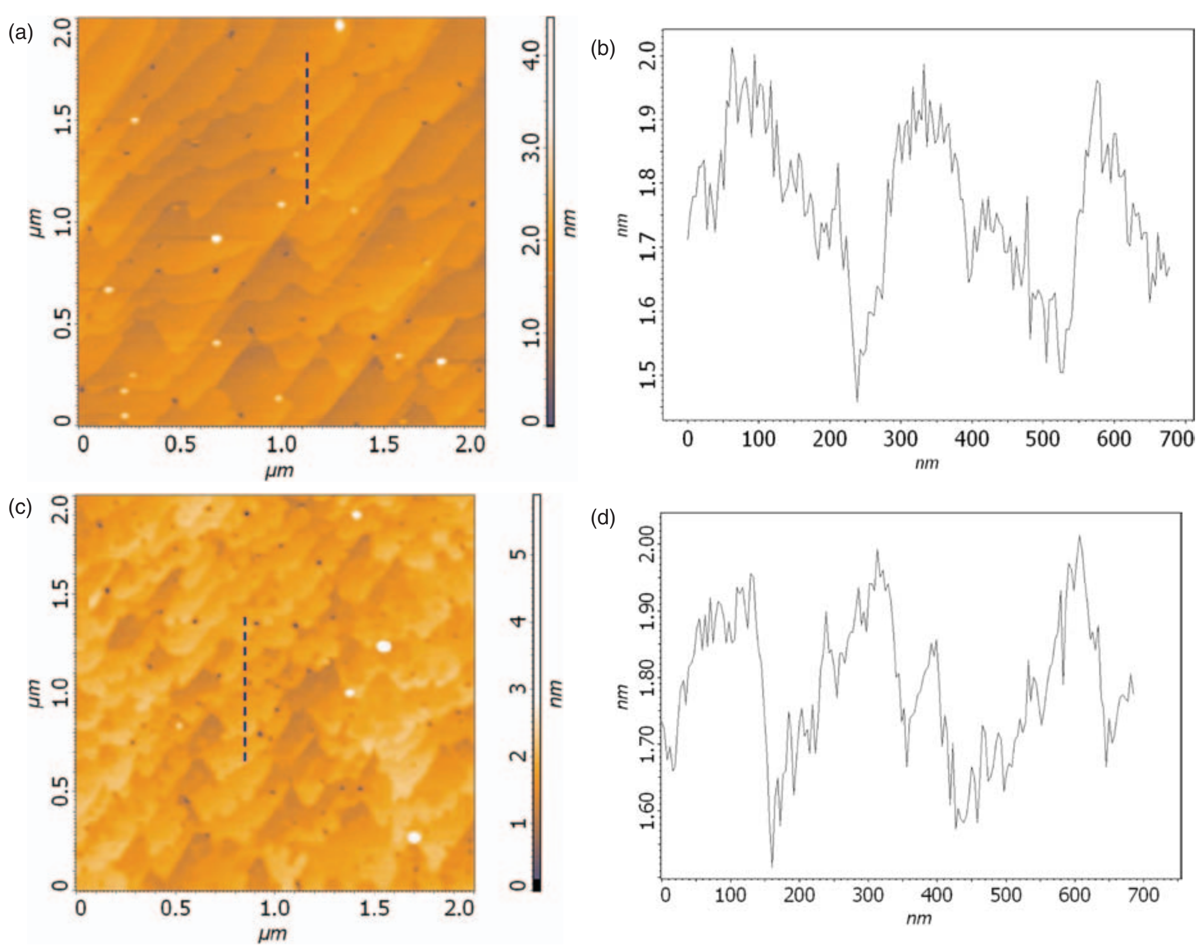

Fig. 4. AFM images (a, c) and height profiles along the lines shown on the AFM images (b, d) for silicon films grown at 750 °C (a, b) and 700 °C (c, d) atop $CrSi_2$ islands.

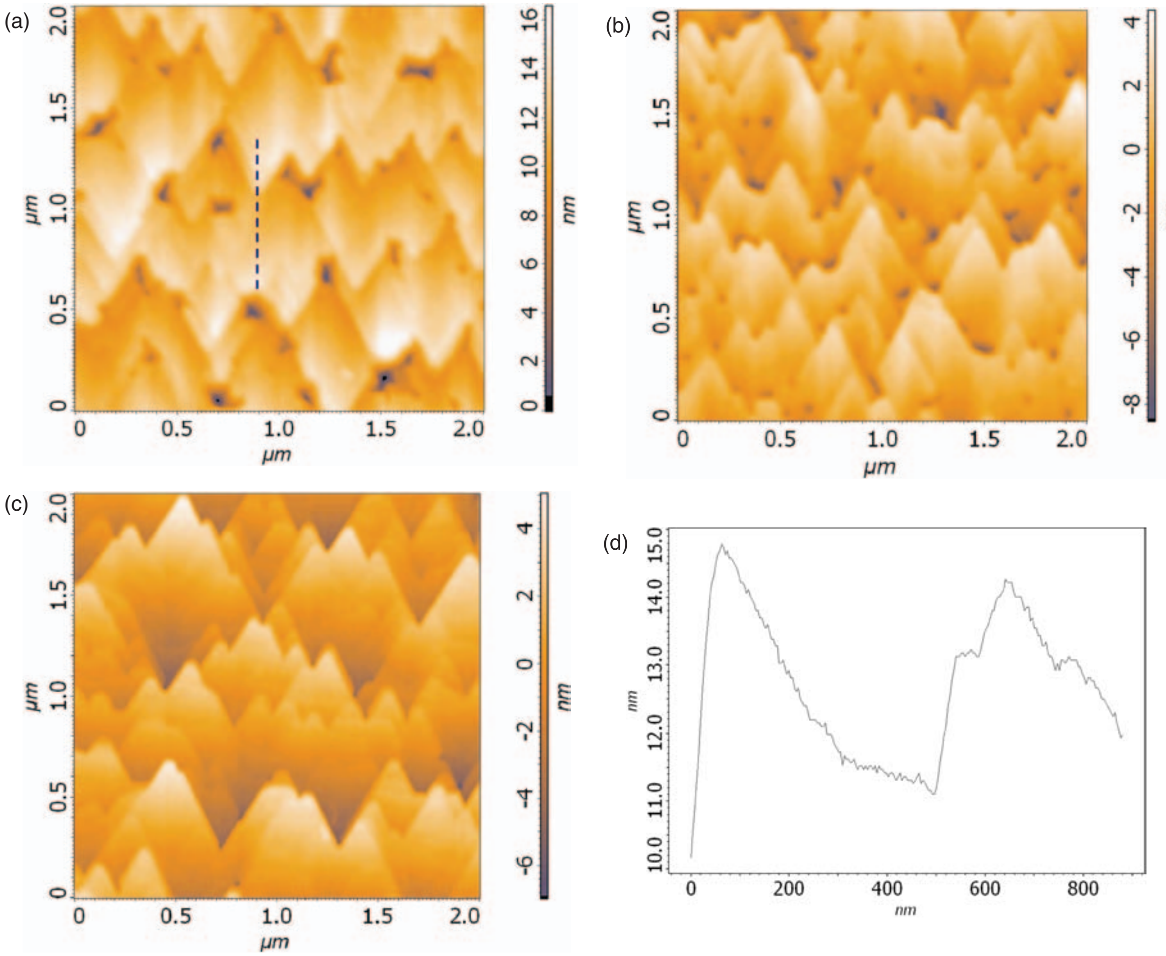

Fig. 5. AFM images of silicon layers with different thicknesses 20 nm (a), 26 nm (b), and 36 nm (c) grown atop $CrSi_2$ islands. (d) Height profile along the line shown on the AFM image for silicon layer 20 nm.

of silicon atoms into the reaction zone due to the surface diffusion mechanism. Silicon deposition at all substrate temperatures and all selected silicon layer thicknesses have resulted in regeneration of Si(111)7×7 surface reconstruction that testifies about epitaxial growth of silicon atop $CrSi_2$ nanosize islands. But maximal intensity of LEED pattern and minimal background was observed at substrate temperature 750 °C (Fig. 3(b)). Investigations of surface morphology by AFM method have shown that the most smooth monocrystalline silicon film with root-mean square roughness of 0.212 nm was obtained at 750 °C (Fig. 4(a)). This growth process corresponds to two monolayer steps on silicon surface (Fig. 4(b)). At lower substrate temperatures the small increase of surface relief and root-mean square roughness up to 0.245 nm at 700 °C (Fig. 4(b)) and 0.296 nm at 650 °C were observed. But step heights were not changed (Fig. 4(c)). As a whole this corresponds to some disordering on a surface due to existence of free atoms and clusters and some density of pinholes with 2–4 nm depths.

Three samples with different Si thickness (20, 26, and 35 nm) atop nanosize $CrSi_2$ islands have been additionally grown in order to determine a minimal silicon thickness needed for a full burying $CrSi_2$ nanocrystallites. Samples have been studied by atomic force microscopy (Fig. 5 (a, b, c)). It is seen that all silicon films have the triangle steps with 300–400 nm sizes, which are usually observed during silicon epitaxial growth on Si(111) substrate. For a minimal Si thickness (20 nm) the maximal pinhole density is observed with depth up to 16 nm. This corresponds to the 2D growth of silicon between silicide islands and points to gradual intergrowth of silicon layers atop $CrSi_2$ islands. Silicon layer thickness 35 nm (Fig. 5(c)) corresponds to the intergrowth stage of silicon crystallites and disappearance of pinholes in silicon film. At larger silicon film thickness (50 nm, Fig. 4(a)) a smoothing of silicon layer surface occurs. So, on this stage a layer-by-layer silicon growth with atomic size steps is observed (Fig. 4(b)) in contrast to the first growth stages, when step heights are 2–4 nm (Fig. 5(d)). Therefore, during an epitaxy of silicon atop $CrSi_2$ nanosize islands silicon growth begins from regeneration of silicon surface and 2D growth on it. After that the 3D silicon growth and overgrowth of silicon islands atop $CrSi_2$ nanosize islands, disappearance of

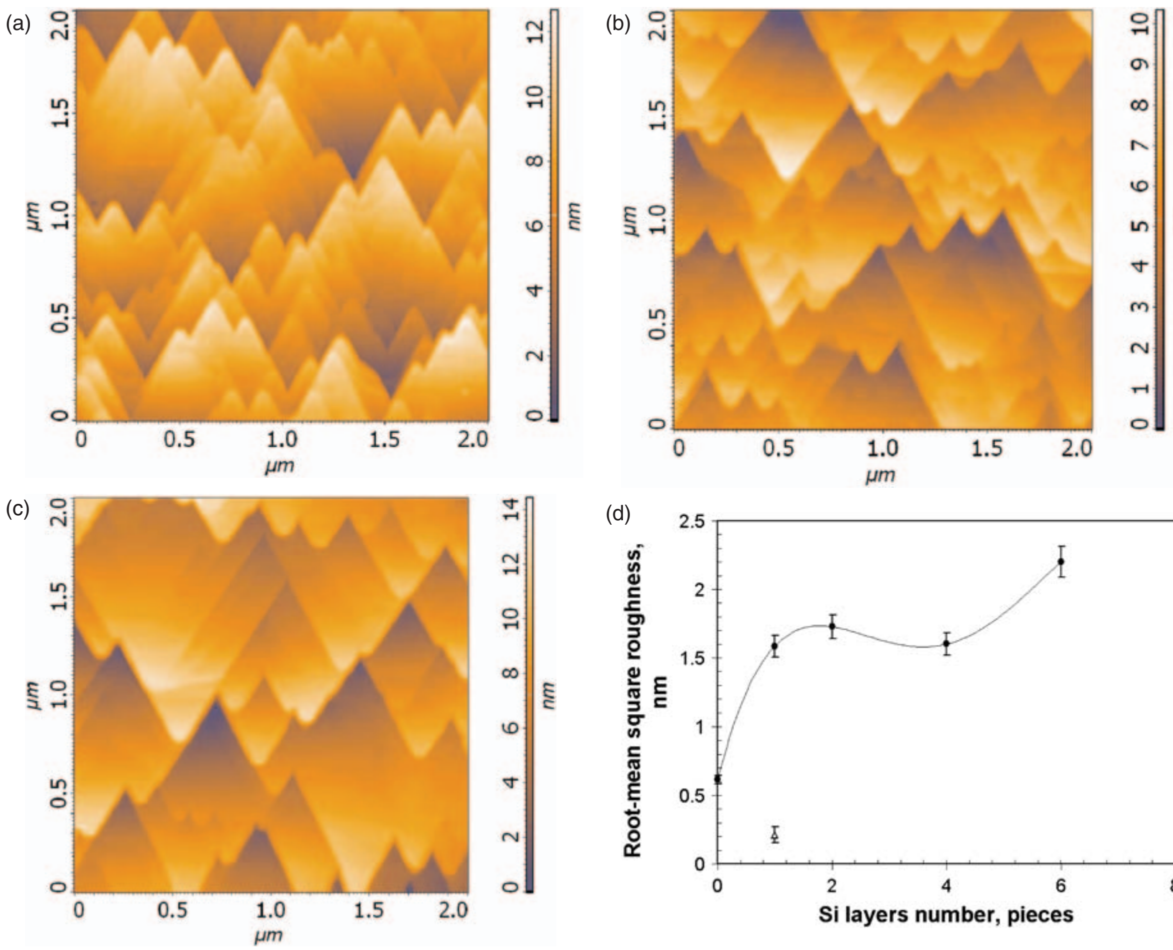

Fig. 6. AFM images for multilayer structures with buried $CrSi_2$ nanocrystallites with different layer numbers: 2(a); 4(b); 6(c). (d) The dependence of root-mean square sample surface roughness from number of grown layers. The value of root-mean square roughness of one buried layer sample with silicon layer thickness 50 nm, grown atop $CrSi_2$ islands at 750 °C, is shown by single triangle.

pinholes and smoothing of growing surface with following layer-by-layer silicon growth as on atomically-clean silicon surface are observed.

For the growth of monolithic silicon structures with few buried layers of $CrSi_2$ nanocrystallites the substrate temperature of 750 °C and silicon layer thickness of 35 nm were selected. Three samples with two, four, and six layers of buried $CrSi_2$ nanocrystallites were grown. Si(111)7×7 patterns were preserved for all cases that corresponds to the formation of monolithic heteronanostructures base on silicon. Morphology of grown layers is presented on Figures 6(a, b, c). It is seen that a film surface consists of triangle crystallites, which have an increased surface relief. However crystallite sizes are about 500 nm that permit to observe a Si(111)7×7 LEED pattern from them. The dependence of root-mean square roughness of grown sample from a value of grown silicon layers and $CrSi_2$ nanocrystallite layers shows on Figure 6(d). The growth of the first silicon layer with thickness 35 nm results in an increase of root-mean square roughness of sample as compared with surface covered by $CrSi_2$ nanosize islands (a value of grown silicon layers equals 0). A situation is conserved up to 4 layers. At 6 layers an increase of roughness is observed. The root-mean square roughness of Si/NC $CrSi_2$/Si(50 nm) sample grown at 750 °C is marked on Figure 6(c) by the single filled triangle. It is seen that at silicon layer thickness 50 nm the multilayer structures will have more smooth surface and good crystalline quality. Therefore, for the further growth of multilayer structures with buried $CrSi_2$ nanocrystallites and atomically smooth surface the silicon thickness about 50 nm would be selected.

4. CONCLUSIONS

The process of self-organization of nanosize islands on Si(111)7×7 surface during Cr reactive deposition epitaxy at 500 °C has been investigated by in situ LEED and DRS methods and ex situ by AFM method. An analysis of differential reflectance data has shown those formed islands are $CrSi_2$ islands with semiconductor optical properties. It was established by DRS and AFM data that Cr deposition (0.016–0.05 nm or 0.2–0.6 Ml) on Si(111)7×7 surface at 500 °C results in the formation of 2D semiconductor $CrSi_2$

islands. At higher Cr thicknesses (0.06–0.07 nm or 0.75–0.9 Ml) the 2D–3D transition in the formation of $CrSi_2$ islands has been observed. $CrSi_2$ islands with high density $(4–5) \cdot 10^9$ cm^{-2}, heights of 1.0–3.0 nm and lateral sizes of 30–50 nm have been formed during this transition. For a growth of silicon layers atop $CrSi_2$ nanosize islands a portion of Cr (0.9 Ml) has been selected. The optimal growth temperature ($T = 750$ °C) for silicon overgrowth at fixed Si thickness (50 nm) has been determined. The minimal Si thickness for the formation of continuous epitaxial silicon film without pinholes at fixed temperature (750 °C) has been found. Monolithic silicon—silicide heterostructures with 2, 4, and 6 layers of $CrSi_2$ nanosize crystallites have been grown. The potential possibility of structure and morphology improvement of grown multilayer heterostructures has shown.

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